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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,996	04/03/2001	Frank Worrell	5201-02906/P2920-1D	4541

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LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/826,996	WORRELL ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 42-81 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Preliminary Amendment as received on 4/3/2001.

Priority

3. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120 as follows:

a) This application is claiming the benefit of a prior filed nonprovisional application under 35 U.S.C. 120, 121, or 365(c). Copendency between the current application and the prior application is required. Applicant's divisional application 09,826,996 was filed on April 3, 2001 and claims priority to U.S. Patent Application 08,661,027 under 35 U.S.C. 120. However, Application 08,661,027 was abandoned on February 1, 2000. According to 35 U.S.C 120:

> "An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States, or as provided by section 363 of this title, which is filed by an inventor or inventors named in the previously filed application shall have the same effect, as to such invention, as though filed on the date of the prior application, **if filed before the patenting or abandonment of or termination of proceedings on the first application** or on an application similarly entitled to the benefit of the filing date of the first application and if it contains or is amended to contain a specific reference to the earlier filed application..."

The examiner asserts that applicant's divisional application was filed after the abandonment of 08,661,027, and consequently, priority is not granted. Therefore, for

purposes of this examination, the effective filing date of the instant application will be the actual filing date (April 3, 2001).

b) An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence of the specification or in an application data sheet (37 CFR 1.78(a)(2) and (a)(5)). The specific reference to any prior nonprovisional application must include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The abstract is objected to because it is too lengthy. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The applicant should remove portions of the abstract that do not relate to the claimed invention (i.e., focus on the fact that compressed and non-compressed routines exists and that branch instructions contain indicators which specify whether or not compression is used in the target routine).

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

7. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. The examiner has been unable to find figures associated with a number of claims. For instance, there is no figure showing a compressed and non-compressed routine and detecting compression/non-compression of a target routine based on an indication in a branch instruction (a flowchart may be helpful). In addition, the examiner has been unable to find storing the current compression mode in a return address register so that when a return is executed, the current compression mode is restored. These features must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 42-81 are rejected under 35 U.S.C. 102(b) as being anticipated by Worrell et al., U.S. Patent No. 5,794,010 (herein referred to as Worrell).

10. Referring to claim 42, Worrell has taught a method for executing a program including a first routine and a second routine in a microprocessor, comprising:

a) executing a branch instruction within said first routine, wherein said branch instruction indicates that said second routine is to be executed via a target address of said branch instruction. See Fig.4D and column 3, line 50, to column 4, line 8.

b) examining an indication specified by said branch instruction, wherein said second routine is determined to be coded using compressed instructions if said indication is in a first state, and wherein said second routine is determined to be coded using non-compressed instructions if said indication is in a second state different than said first state. See column 3, lines 18-26, and column 11, lines 35-48.

11. Referring to claim 43, Worrell has taught a method as described in claim 42. Worrell has further taught that said branch instruction is a call instruction, wherein said executing includes storing a return address. See column 3, lines 28-33.

12. Referring to claim 44, Worrell has taught a method as described in claim 42. Worrell has further taught that said indication comprises a bit and said first state comprises said bit being set. See Fig.4D, field 94, and column 11, lines 35-48.

13. Referring to claim 45, Worrell has taught a method as described in claim 44. Worrell has further taught that said second state comprises said bit being clear. See Fig.4D, field 94, and column 11, lines 35-48.

14. Referring to claim 46, Worrell has taught a method as described in claim 42. Worrell has further taught storing said indication in a program counter within said microprocessor. See column 11, lines 48-50.

15. Referring to claim 47, Worrell has taught a method as described in claim 42. Worrell has further taught that said indication serves as a compression mode for said second routine. See Fig.4D, field 94, and column 11, lines 35-48.

16. Referring to claim 48, Worrell has taught a method as described in claim 47. Worrell has further taught decompressing instructions from said second routine if said compression mode indicates compressed. Clearly, if instructions are compressed, they must be decompressed. A decompressor, as seen in Fig.2 for instance, would be the component used to perform such decompression.

17. Referring to claim 49, Worrell has taught a method as described in claim 43. Worrell has further taught executing a return instruction at completion of said second routine, wherein said return instruction indicates said return address. See column 3, lines 33-35, and column 19, lines 26-29.

18. Referring to claim 50, Worrell has taught a method as described in claim 49. Worrell has further taught examining a second bit within said return address, wherein

said first routine is determined to be coded using compressed instructions if said second bit is in a first state, and wherein said first routine is determined to be coded using non-compressed instructions if said second bit is in a second state different than said first state. See column 3, lines 28-35, and claim 18.

19. Referring to claim 51, it should be noted that the apparatus of claim 51 performs the method of claim 42. Consequently, claim 51 is rejected for the same reasons set forth in the rejection of claim 42.

20. Referring to claim 52, Worrell has taught an apparatus as described in claim 51. Furthermore, it should be noted that the apparatus of claim 52 performs the method of claim 43. Consequently, claim 52 is rejected for the same reasons set forth in the rejection of claim 43.

21. Referring to claim 53, Worrell has taught a microprocessor comprising:

a) a mode detector configured to detect a compression mode of a target routine in response to a branch instruction, wherein said branch instruction specifies an address and the compression mode of said target routine. See column 3, line 50, to column 4, line 8. Note that a mode detector would detect the value of the compression mode bit and that a call instruction provides a target address.

b) an execution unit coupled to said mode detector, wherein said execution unit is configured to execute compressed instructions if said compression mode indicates compressed, and wherein said execution unit is configured to execute non-compressed instructions if said compression mode indicates non-compressed. See column 3, line 50, to column 4, lines 8.

22. Referring to claim 54, Worrell has taught a microprocessor as described in claim 53. Furthermore, it should be noted that the microprocessor of claim 54 performs the method of claim 44. Consequently, claim 54 is rejected for the same reasons set forth in the rejection of claim 44.

23. Referring to claim 55, Worrell has taught a microprocessor as described in claim 54. Furthermore, it should be noted that the microprocessor of claim 55 performs the method of claim 44. Consequently, claim 55 is rejected for the same reasons set forth in the rejection of claim 44.

24. Referring to claim 56, Worrell has taught a microprocessor as described in claim 53. Worrell has further taught a storage device coupled to the mode detector and configured to store a compression enable indicator, wherein the mode detector is configured to detect the compression mode responsive to the compression enable indicator. See column 4, lines 9-22.

25. Referring to claim 57, Worrell has taught a microprocessor adapted to operate on compressed instructions in addition to non-compressed instructions, wherein the microprocessor comprises:

a) a mode detector configured to receive a branch instruction specifying a compression mode indication, the mode detector configured to provide a compression mode signal in response to the compression mode indication of the branch instruction. See claim 17.

b) an execution unit configured to execute non-compressed instructions, wherein the execution unit is configured to update a current compression mode in response to the compression mode signal provided from the mode detector. See claim 17.

c) an instruction decompressor coupled to provide non-compressed instructions to the execution unit, wherein the instruction decompressor is configured to selectively decompress received instructions into non-compressed instructions depending on the current compression mode. See Fig.2 and claim 17.

26. Referring to claim 58, Worrell has taught a microprocessor as described in claim 57. Furthermore, it should be noted that the microprocessor of claim 58 performs the method of claim 43. Consequently, claim 58 is rejected for the same reasons set forth in the rejection of claim 43.

27. Referring to claim 59, Worrell has taught a microprocessor as described in claim 58. Worrell has further taught a return address register for storing said return address, wherein the return address register is configured to store the current compression mode when the execution unit executes the call instruction and to restore the current compression mode to the program counter upon execution of a subroutine return instruction. See column 3, lines 26-35.

28. Referring to claim 60, Worrell has taught a microprocessor as described in claim 58. Worrell has further taught that said compression mode indication is a least significant bit of a target address. See column 7, lines 6-11.

29. Referring to claim 61, Worrell has taught a method for executing a program including a first routine and a second routine in a microprocessor, comprising:

a) executing a branch instruction within said first routine, wherein said branch instruction indicates that said second routine is to be executed via a target address of said branch instruction, and wherein an operand of the branch instruction includes an indication. See

column 3, line 50, to column 4, line 8. Also, see Fig.4D and note that the EX field is the indicator and is an operand of the branch instruction.

b) examining the indication, wherein said second routine is determined to be coded using compressed instructions if said indication is in a first state, and wherein said second routine is determined to be coded using non-compressed instructions if said indication is in a second state different than said first state. See column 3, lines 18-26, and column 11, lines 35-48.

30. Referring to claim 62, Worrell has taught a method as described in claim 61. Worrell has further taught that said operand is an immediate operand. See Fig.4D. It should be noted that there are generally either immediate operands, which are immediate data stored within the instruction for immediate use by the instruction, or register operands, which are references to registers that hold data required by the instruction. Clearly, the compression indication is an immediate operand because it is stored immediately within the instruction (and not in some register referenced by the instruction).

31. Referring to claim 63, Worrell has taught a method as described in claim 61. Worrell has further taught selectively decompressing instructions within said second routine responsive to said indication. Clearly, if instructions are compressed, then they must be decompressed. The decompressor shown in Fig.2, for instance, would be a component which performs such decompressing.

32. Referring to claim 64, Worrell has taught a method as described in claim 61. Worrell has further taught updating a current compression mode responsive to the indication. See claim 17.

33. Referring to claim 65, Worrell has taught a method as described in claim 61. Furthermore, claim 65 is rejected for the same reasons set forth in the rejection of claim 43.

34. Referring to claim 66, Worrell has taught a method as described in claim 65. Furthermore, claim 66 is rejected for the same reasons set forth in the rejection of claim 49.

35. Referring to claim 67, it should be noted that the apparatus of claim 67 performs the method of claim 61. Consequently, claim 67 is rejected for the same reasons set forth in the rejection of claim 61.

36. Referring to claim 68, Worrell has taught an apparatus as described in claim 67. Furthermore, it should be noted that the apparatus of claim 68 performs the method of claim 62. Consequently, claim 68 is rejected for the same reasons set forth in the rejection of claim 62.

37. Referring to claim 69, Worrell has taught an apparatus as described in claim 67. Furthermore, it should be noted that the apparatus of claim 69 performs the method of claim 63. Consequently, claim 69 is rejected for the same reasons set forth in the rejection of claim 63.

38. Referring to claim 70, Worrell has taught an apparatus as described in claim 67. Furthermore, it should be noted that the apparatus of claim 70 performs the method of claim 64. Consequently, claim 70 is rejected for the same reasons set forth in the rejection of claim 64.

39. Referring to claim 71, Worrell has taught an apparatus as described in claim 67. Furthermore, it should be noted that the apparatus of claim 71 performs the method of

claim 65. Consequently, claim 71 is rejected for the same reasons set forth in the rejection of claim 65.

40. Referring to claim 72, Worrell has taught an apparatus as described in claim 71. Furthermore, it should be noted that the apparatus of claim 72 performs the method of claim 66. Consequently, claim 72 is rejected for the same reasons set forth in the rejection of claim 66.

41. Referring to claim 73, the microprocessor of claim 53 includes each of the components in the microprocessor of claim 73. Consequently, claim 73 is rejected for the same reasons set forth in the rejection of claim 53.

42. Referring to claim 74, Worrell has taught an apparatus as described in claim 73. Furthermore, it should be noted that the microprocessor of claim 74 performs the method of claim 62. Consequently, claim 74 is rejected for the same reasons set forth in the rejection of claim 62.

43. Referring to claim 75, Worrell has taught an apparatus as described in claim 73. Furthermore, it should be noted that the microprocessor of claim 75 performs the method of claim 63. Consequently, claim 75 is rejected for the same reasons set forth in the rejection of claim 63. That is, note the decompressor of Fig.2 and realize that it would be used to decompress compressed instructions.

44. Referring to claim 76, Worrell has taught a microprocessor as described in claim 73. Furthermore, the microprocessor of claim 76 performs the method of claim 65. Consequently, claim 76 is rejected for the same reasons set forth in the rejection of claim 65.

45. Referring to claim 77, Worrell has taught a microprocessor as described in claim 76. Furthermore, the microprocessor of claim 77 performs the method of claim 66. Consequently, claim 76 is rejected for the same reasons set forth in the rejection of claim 66.

46. Referring to claim 78, Worrell has taught a microprocessor adapted to operate on compressed instructions in addition to non-compressed instructions, wherein the microprocessor comprises:

a) a mode detector configured to receive a branch instruction having an operand including a compression mode indication, the mode detector configured to detect a compression mode in response to the compression mode indication of the branch instruction. See claim 17 and Fig.4D (note the compression indicator operand field 94).

b) an execution unit configured to execute non-compressed instructions, wherein the execution unit is configured to update a current compression mode in response to the compression mode signal provided from the mode detector. See claim 17.

c) an instruction decompressor coupled to provide non-compressed instructions to the execution unit, wherein the instruction decompressor is configured to selectively decompress received instructions into non-compressed instructions depending on the current compression mode. See Fig.2 and claim 17.

47. Referring to claim 79, Worrell has taught a microprocessor as described in claim 78. Furthermore, it should be noted that the microprocessor of claim 79 performs the method of claim 62. Consequently, claim 79 is rejected for the same reasons set forth in the rejection of claim 62.

48. Referring to claim 80, Worrell has taught an apparatus as described in claim 78. Furthermore, it should be noted that the microprocessor of claim 80 performs the method of claim 65. Consequently, claim 80 is rejected for the same reasons set forth in the rejection of claim 65.

49. Referring to claim 81, Worrell has taught an apparatus as described in claim 78. Furthermore, it should be noted that the microprocessor of claim 81 performs the method of claim 66. Consequently, claim 81 is rejected for the same reasons set forth in the rejection of claim 66.

Conclusion

50. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Tan et al., U.S. Patent No. 6,189,090, has taught a processor which operates in both 16 and 32-bit instruction modes. JUMP and CALL instructions are coded to indicate the processor mode. When a CALL is executed, the current mode is stored on a stack so that when a RETURN is executed, the mode may be restored.

Yokota, U.S. Patent No. 5,652,852, has taught a processor for discriminating between compressed and non-compressed program code. More specifically, an instruction is used to indicate the compression mode, and if it indicates compression, then the corresponding instructions must be expanded (decompressed).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
February 1, 2005